REMARKS

Favorable reconsideration of this application in light of the following remarks is respectfully requested. Of the pending claims, claims 1-3 and 9-12 are under consideration. Claims 2 and 9 are amended by the present Amendment.

In the Office Action dated August 23, 2004, claim 2 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite and claims 1-3 and 9-12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 5,994,743 to Masuoka in view of U.S. Patent 6,020,231 to Wang. The rejection is traversed for the reasons stated below.

The Rejection of Claim 2

In the Office Action, claim 2 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Applicants have amended claim to 2 to more appropriately claim an embodiment of the disclosure. Accordingly, Applicants respectfully submit that claim 2 satisfies 35 U.S.C. § 112, second paragraph.

The Rejection of Claims 1-3

In the Office Action, claims 1-3 and 9-12 were rejected under 35 U.S.C. §103(a) as being unpatentable over Masuoka in view of Wang. Applicants respectfully traverse this rejection.

The Office Action asserts that Masuoka shows the elements recited in independent claims 1 and 9 except that Masuoka discloses a method opposite to what is recited in claims 1 and 9. In particular, Masuoaka discloses forming a transistor such that the width of the sidewall structure adjacent to the PMOS transistor is narrower than the width of the sidewall structure adjacent to the NMOS transistor. This is in contrast to claim 1, which recites that the width of a first single layer sidewall structure adjacent to the NMOS transistor gate structure is formed to be less than the width of a second single layer sidewall structure adjacent to the PMOS transistor gate structure.

In addition to Masuoka disclosing a method opposite to what is recited in claim 1 of the instant invention, Masuoka does not disclose etching an initial single layer sidewall structure. Rather, Masuoka etches a processed dual layer sidewall structure comprising damaged layer 39 and sidewall layer 33.

In particular, Masuoka forms the dual layer sidewall structure by ion implanting BF_2^+ at a 45 degree angle away from normal using low energy (5 KeV) so as to form damaged layer 39 adjacent the sidewall layer 33. See Masuoka col. 6, lines 19-24. Masuoka's dual layer sidewall structure is not the initial single layer structure shown in Fig. 2(c). Indeed, Masuoka highlights the distinct two layers as is shown in Fig. 2(e) by the sidewall having multiple layers.

According to Masuoka, forming damaged regions 39 is necessary in order to obtain the appropriate etch rate ratio required to etch the sidewall structure with a wet HF etch. See Matsuoka col. 6, lines 28-35. Specifically, Masuoka states that etch rate of wet HF etching of un-damaged SiO_2 is 4 nm/min, but becomes as much as twenty

times that for the damaged layers 39 of the sidewall spacers. See Masuoka col. 6, lines 30-33. Masuoka must form damaged layers in order to have proper etch controllability. See Masuoka col. 6, lines 33-35.

In contrast, claim 1 of the instant invention recites etching *the initial single layer sidewall structure* adjacent to the NMOS transistor. Etching a dual layer sidewall structure (i.e., a damaged layer 39 and a sidewall layer 33) where the damaged layer is preferentially wet etched with respect to the undamaged layer is not the same as etching an initial single layer sidewall structure because the dual layer sidewall spacer having a damaged layer is no longer the initial single layer sidewall structure. Therefore, Applicants respectfully submit that Masuoka does not disclose the elements recited in claim 1. Moreover, Wang does not correct the deficiencies of Masuoka with respect to claim 1.

It is to be noted that Masuoka explicitly states that the 45 degree angle low energy implant is used only to form damaged layer 39. The BF_2^+ is not used to dope regions adjacent the gate because the implant energy is too low. See Masuoka col. 6, lines 24-27.

Accordingly, Applicants respectfully request that the Examiner reconsider and withdraw the rejection of claim 1 under 35 U.S.C. §103(a). Applicants futher submit that claim 1 is in condition for allowance.

In addition, claims 2 and 3 depend from claim 1, and thus, are allowable for at least the same reasons that claim 1 is allowable, as well as for their additional

recitations. Therefore, Applicants respectfully submit that claims 2 and 3 are also allowable over Masuoka in view of Wang.

With respect to claims 9-12, Applicant's have amended claim 9 to include that LDD regions are formed adjacent to the first and second transistor gate stacks. This is in contrast to Masuoka who explicitly limits forming LDD structures in only the NMOS device. For example, Masuoka states that "the nMOSFET is formed of the LDD structure and the pMOSFET is formed of the single drain structure." See Masuoka col. 6, lines 50-52.

Indeed, Masuoka teaches away from forming LDDs adjacent both transistor gate stacks by specifically using only two photolithography processes during fabrication. See Masuoka col. 3, lines 28-32. As disclosed by Masuoka, the first photolithography mask is used to form high concentration n-type source and drain regions 36 in the nMOSFET (see Masuoka col. 6, lines 10-14), the n-type LDD structures 31 having already been formed using the gate electrode 26 as a mask[1] (see Masuoka col. 5, line 62 through col. 6, line 1). The second photolithography mask is used to form and etch the damaged layer 39 and to form p+-type source and drain regions 41. See Masuoka col. 6, lines 16-41. As such, there is no opportunity for Masuoka to form LDDs adjacent to the pMOSFET gate because this would require an additional mask. Because Masuoka intentionally limits the number of photolighography steps, Masuoka does not perform an implant to form LDD structures adjacent the gate electrode 27 of the pMOSFET.

[1] It is to be noted that structures 32 are not LDD structures. Rather, they are counter doped regions and are of the same dopant used to form regions 31.

Additionally, Masuoka states that LDDs for the pMOSFET are unnecessary and that the counter doped regions 32 are inverted by heavily p+-doping to form the source and drain regions 41. See Masuoka col. 6, lines 38-41.

As such, Applicants respectfully submit that Masuoka explicitly teaches away from forming LDD regions adjacent the first transistor gate stack and adjacent the second transistor gate stack. Moreover, Wang does not correct the deficiencies of Masuoka with respect to claim 9. Accordingly, Applicants respectfully request that the Examiner reconsider and withdraw the rejection of claim 9 under 35 U.S.C. §103(a). Applicants futher submit that claim 9 is in condition for allowance.

In addition, claims 10-12 depend from claim 9, and thus, are allowable for at least the same reasons that claim 9 is allowable, as well as for their additional recitations. Therefore, Applicants respectfully submit that claims 10-12 are also allowable over Masuoka in view of Wang.

In view of the foregoing amendments and remarks, Applicants respectfully request the reconsideration of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any required fees to the Texas Instruments Incorporated Deposit Account 20-0668.

Respectfully submitted,

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